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Question n. 1

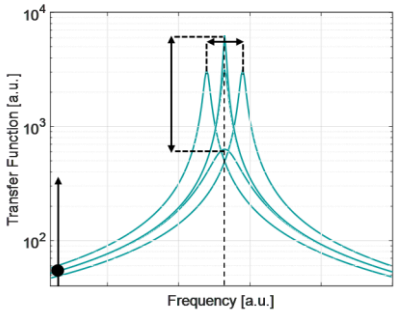
Consider a gyroscope designed for a mode-split architecture. Discuss the sources of variability from part to part and vs environmental conditions, and try to quantify their effects on the scale factor for typical operating conditions.

Gyroscopes operating in mode-split conditions show an intended difference $\Delta\omega_{MS}$ between the drive- and sense-mode resonance, usually set at 2-3 times the required bandwidth. This yields a few interesting aspects and one drawback.

Concerning the requests of this question, the interesting aspects are that:

- The sensitivity (scale-factor), given by the formula:
$$SF = 2\frac{V_{ROT}}{C_F}\frac{C_S}{g}\frac{x_D}{\Delta\omega_{MS}}$$
becomes rather independent of the quality factor of the sense mode, so of its possible variability in temperature (Q goes with one over the square root of T) and from part to part. Residual variability in the sensitivity can be given by the drive-mode Q, which would affect the displacement x_D. However, an AGC in the drive loop is sufficient to compensate this issue;
- The process variability that affects the electromechanical parameters ($C_S, g, \Delta\omega_{MS}$) determines a part-to-part variability, which requires an initial calibration. However, C_S and g can be assumed rather constant over temperature;
- $\Delta\omega_{MS}$ shows itself a dependence on temperature which is due to the temperature coefficient of the Young's modulus, inducing frequency variations proportional to the absolute value of the frequency itself at a reference temperature, and thus different for the two modes:
$$\omega_d = \omega_{d,0}(1 + \alpha\Delta T)$$
$$\omega_s = \omega_{s,0}(1 + \alpha\Delta T)$$
$$\Delta\omega_{MS} = (\omega_{s,0} - \omega_{d,0})(1 + \alpha\Delta T) = \Delta\omega_{MS,0}(1 + \alpha\Delta T)$$
(where α is -30 ppm/K). The result, from a quantitative point of view, is anyway much better than for mode-matching operation, as the resulting drift of the scale factor in temperature turns out to be within less than 1% across the typical temperature range.

Effects of the change in the quality factor and mode-split value on the scale factor are qualitatively represented in the figure, which shows how the gain at a certain nominal distance from resonance is not impacted significantly by changes of the sense-mode transfer function or by small changes in the mode-split value.



One disadvantage of operating in mode-split conditions is that input-referred electronic noise $\sqrt{S_{V_n,acc}}$ increases, as the scale-factor is generally lower than for mode-matched operation. Additionally, the variations in the scale-factor from part to part discussed above have a direct effect on input referred electronic noise (originating from the amplifier noiseS_{V_n}) which may itself change from part to part:

$$\sqrt{S_{V_n,acc}} = \frac{\sqrt{2S_{V_n}}\left(1 + \frac{C_P}{C_F}\right)}{SF}$$

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Question n. 2

Design an in-plane MEMS accelerometer to match the specifications indicated in the Table, and the corresponding readout chain (*hint: follow the standard procedure that we used during exercise lectures*).

Motivate your design choices, help yourself with suitable drawing, and, while you size your device and circuit, fill-in the second Table below.

Process thickness	30 µm
Minimum gap	1.5 µm
Full-scale range (1% linearity error)	± 80 g
Resolution	20 µg/√Hz
Maximum consumption	10 mA
MOS k_n parameter	1 mA/V^2
IC supply voltage	± 5 V
Area	1 mm x 1 mm
Bandwidth	400 Hz
Parasitic capacitance	5 pF
Minimum IC capacitance	40 fF

Physical Constants

$\varepsilon_0 = 8.85\ 10^{-12}$ F/m

$\rho_{Si} = 2350$ kg/m^3 ;

$k_b = 1.38\ 10^{-23}$ J/K;

T = 300 K;

Resonance frequency	11.5 kHz
Mass	35 nkg
Stiffness	189 N/m
Quality factor	1.8
Electrostatic stiffness	-4.4 N/m
Scale-factor (sensitivity)	62.5 mV/g
Sense capacitance (single-ended)	200 fF
Amplifier noise	7 nV/√
Transistor g_m parameter	1.3 mA/V

There are a few parameters that are very straightforward to calculate.

The first one is the optimal scale factor, which simply turns out to be:

$$SF = 2\frac{V_{ROT}}{C_F}\frac{C_0}{g}\frac{1}{\omega_0^2} = \frac{V_{DD}}{FSR} = \frac{\pm 5\ V}{\pm 80\ g} = 62.5\frac{mV}{g}$$

In the formula above V_{ROT} is e.g. the amplitude of a modulated signal which will be later demodulated in the readout chain. It can be for the sake of optimization set at V_{DD} itself.

The second one is the maximum displacement, as the linearity error is known. It is given as:

$$x_{max} = g\sqrt{\epsilon_{lin}} = 1.5\ \mu m\sqrt{0.01} = 150\ nm$$

From which we can immediately calculate the resonance frequency in operation ω_0, given by:

$$x_{max} = \frac{FSR}{\omega_0^2} \rightarrow\ \omega_0 = \sqrt{\frac{FSR}{x_{max}}} = \sqrt{\frac{80 \cdot 9.8\ m/s^2}{150\ nm}} = 72.3\frac{krad}{s} \rightarrow f_0 = 11.51\ kHz$$

To get the desired bandwidth, it will be sufficient to filter the chain with a 400 Hz LPF.

For what concerns the readout chain, it is wise to minimize the feedback capacitance of the front-end stage: indeed, for the same scale-factor, this allows also to minimize the rest MEMS capacitance, and thus the overall MEMS area. We thus choose $C_F = 40\ fF$ and we can find the single-ended MEMS capacitance that copes with the required scale-factor:

$$C_0 = \frac{SF}{2\frac{V_{ROT}}{C_F}\frac{1}{g}\frac{1}{\omega_0^2}} = 200\ fF$$

(take care: the SF shall be here expressed in V/(m/s^2) and not in V/g, so to retrieve the correct value of the capacitance).

After estimating the mass value as:

$$m = \rho \cdot h \cdot A_{eff} = 2350\frac{kg}{m^3} \cdot 30\mu m \cdot (1mm)^2 \cdot 0.5 = 35\ nkg$$

(the factor 0.5 accounts for the holes required to insert the readout plates), we can now check the value of the electrostatic stiffness and of the elastic stiffness by comparing:

$$k_{elec} = -\frac{2C_0V_{DD}^2}{g^2} = -4.4\ \frac{N}{m}$$

$$k_{tot} = \omega_0^2 \cdot m = 184.4\ \frac{N}{m}$$

Which implies that the required mechanical stiffness is $k_{mec} = 188.8\frac{N}{m}$.

The thermomechanical noise contribution satisfies noise requirements (assuming a 50% power density split between device and electronics) if:

$$NEAD = \sqrt{\frac{4k_BT\omega_0}{mQ}} = \frac{20}{\sqrt{2}}\frac{\mu g}{\sqrt{Hz}} \rightarrow Q = 1.8$$

At this point, we can check whether the current budget is enough to cope with this noise distribution:

$$\sqrt{S_{V_n}\left(1+\frac{C_P}{C_F}\right)^2} = \frac{20}{\sqrt{2}}\frac{\mu g}{\sqrt{Hz}} \cdot SF = 882\frac{nV}{\sqrt{Hz}} \rightarrow \sqrt{S_{V_n}} = 7\ \frac{nV}{\sqrt{Hz}}$$

Which implies that the gm parameter of the transistors shall be:

$$\sqrt{S_{V_n}} = \sqrt{2 \cdot 2 \cdot \frac{4k_BT}{g_m}\gamma} \rightarrow g_m = 1.3\frac{mA}{V}$$

The current required by each MOS transistor is thus:

$$I_{MOS} = \frac{g_m^2}{k_n} = 1.8\ mA$$

The total front-end consumption is 4 times the value above, and fits within some reasonable margin (to account for the consumption of other stages) in the total current budget.

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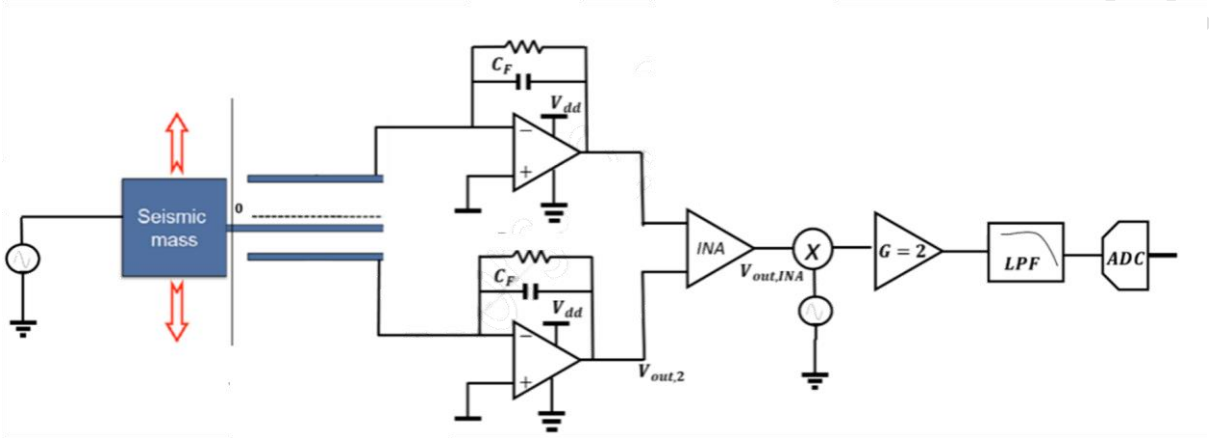
A sample readout chain which can be adopted is shown below. We will choose the modulation frequency at at least 10 times the resonance (e.g. 150 kHz), and the feedback resistance accordingly to let this frequency pass properly through the chain. The LPF will be set at 400 Hz, as required by the specifications. The n. of bit of the ADC shall cope with the resolution, implying that

$$DR = 20\log_{10}\frac{\pm 80g}{20\frac{\mu g}{\sqrt{Hz}}\sqrt{400\ Hz}} = 112\ dB = 400000$$

$$N_{bit} = \log_2 400000 = 18.6 \rightarrow 19\ bit$$



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Question n. 3

Design the pixel of a 3T CMOS image sensor to match the specifications given in the Table aside (*hint: follow the standard procedure that we used during exercise lectures*).

Motivate your design choices, help yourself with suitable drawing, and, while you size your device and circuit, fill-in the second Table below.

Resolution @ min F#, 550 nm	2 µm
F# range	1.4 – 16
Min/Max integration time	0.5 ms – 5 s
Maximum DR	65 dB
Time for which Max DR is valid	50 ms
Max SNR	42 dB
Supply voltage	2.5 V
Sensor capacitance per unit area	0.4 fF/(µm)^2
MOS capacitance per unit area	0.5 fF/(µm)^2
Minimum total area of 1 MOS	500 nm x 500 nm

Physical Constants

ε_{Si} = 11.7*8.85 10^{-12} F/m

k_b = 1.38 10^{-23} J/K;

T = 300 K;

q = 1.6 10^{-19} C

Full well charge (n. of electrons)	25220
Integration Capacitance	1.6 fF
Estimated pixel size	2 µm
Photodiode size	1.8 µm
MOS size	(500 nm)^2
Need for microlenses? (Yes/No)	No
Maximum dark current	0.83 fA
ADC n. of bits	9

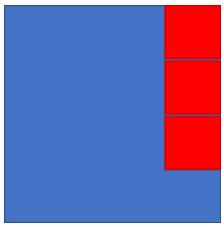
The first parameter that we can easily check is the resolution, and thus the pixel size. Initially, we evaluate the diffraction effects at 550 nm for the minimum F number:

$$d_{Airy} = 2.44 \cdot \lambda \cdot F_{\#} = 1.8\ \mu m$$

Which implies that we can effectively cope with the specified resolution, provided that the pixel size is itself compatible. We thus choose a pixel size which is itself:

$$d_{pix} = 2\ \mu m$$

Assuming to use MOS transistors with minimum area, they will leave a residual area for the photodiode (see the picture aside) equal to:



$$A_{PD} = A_{pix} - 3 \cdot A_{MOS} = (2\ \mu m)^2 - 3 \cdot (500\ nm)^2 = (1.8\ \mu m)^2$$

Meaning that the area taken up by the transistors is minimal. Micro-lenses are not mandatory in this case. Note that while some space for interconnections might be required as well, it is also true that portions of the MOS can overlap one another, so the approximation done here is assumed valid.

Once the photodiode area is known, we can use the maximum SNR parameter to verify the number of electrons that can fit inside the photodiode well:

$$SNR_{max} = 20\log_{10}\sqrt{N_{el,max}} \rightarrow N_{el,max} = \left(10^{44/20}\right)^2 = 25220\ e^-$$

We know that this number is related to the integration capacitance and the supply voltage, from which we can thus evaluate the integration capacitance:

$$Q_{max} = q \cdot N_{el,max} = C_{int}V_{DD} \rightarrow C_{int} = 1.6\ fF$$

Let us check whether with the sized photodiode we can match this capacitance:

$$C_{PD} = 0.4\frac{fF}{\mu m^2}\ (1.8\ \mu m)^2 = 1.3\ fF \quad C_{MOS} = 0.5\frac{fF}{\mu m^2}\ (0.5\ \mu m)^2 = 0.12\ fF$$

The total integration capacitance almost matches the required value. We thus assume this sizing reasonable.

We set a value for the dark current such that at the largest integration time $t_{int,maxDR}$ for which the maximum DR remains valid, the dark current is just equal to the reset noise:

$$k_BT\ C_{int} = q\ i_d\ t_{int,maxDR} \rightarrow i_d = 0.83\ fA$$

And finally, we decide the number of bits of the ADC from the DR requirement:

$$\left(\frac{V_{DD}\cdot C_{int}}{2^{N_{bit}}\sqrt{12}}\right)^2 \leq k_BT\ C_{int} \rightarrow N_{bit} = 8.8 \rightarrow N_{bit} = 9$$

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