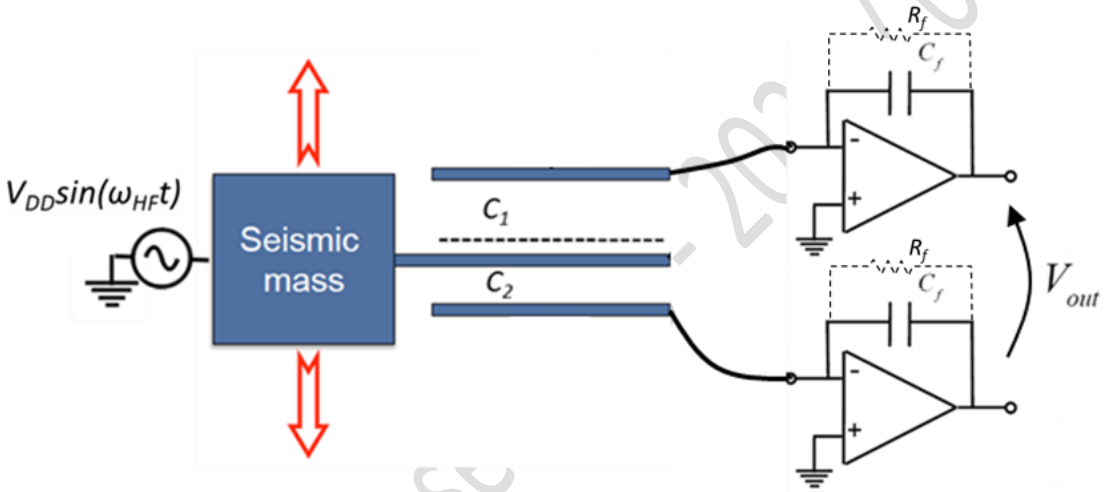
Last Name __DIFFICI___ **Given Name** __LINO____ **ID Number** __20220117__

Question n. 1

Draw a typical front-end of an electronic capacitive sensing interface for a generic differential MEMS sensor, whose input signal is modulated around a frequency f_0. Discuss in detail how to optimize the passive components sizing of the stage. Describe also the criteria to size the stage current consumption. Finally, comment on the effects of spread and drifts of the passive components on the MEMS sensor performance.

There are various situations where the signal at the front-end input of a MEMS system is modulated. It is e.g. the case of gyroscopes or magnetometers, where modulation occurs at the drive frequency or current excitation frequency respectively. It is also the case of accelerometers, where a modulation can be on purpose applied as an AC signal to the rotor. This is the situation depicted as an example below (in case of gyroscopes or magnetometers, the rotor is not modulated).



Whatever the case, the motional current exiting the differential MEMS capacitances occurs at a frequency f_0, usually in the 20-100 kHz range.

Taking into account constraints of noise, repeatability and gain, the best choice to transduce such a current into a voltage is a pair of charge amplifier, each having a feedback network formed by the parallel of a resistance R_F and a capacitance C_F. In particular, the sizing of these passive components can be done by accounting for the following three rules of thumb:

- the pole introduced by R_F and C_F shall be at least one decade (two is even better) before the operating frequency f_0, so to guarantee operation in charge amplifier mode;
- the stage gain, given by $1/(2\pi f_0 C_F)$, shall maximize the output, approaching the voltage supply for an input corresponding to the FSR, at the same time avoiding saturation;
- noise introduced by R_F shall be in line or negligible compared to the other noise sources.

Though we have set three conditions to size two components only, usually by choosing a large enough resistance, e.g. implemented through MOS transistors in off state, the first and last conditions are simultaneously met, while the second condition is used to size the capacitance.

The front-end will be then completed typically by an INA to turn the signal into single-ended, and by demodulation, filtering and digitization stages.

An additional relevant noise source in the system is represented by the amplifier input pair. Giving the dependence of the noise on the current drawn by the amplifiers, e.g. in saturation mode:

$$S_{V_n} = \frac{4k_B T\gamma}{g_m} = \frac{4k_B T\gamma}{\sqrt{k_n\, i_{MOS}}}$$

it is clear that to minimize noise we are required to increase the current. As this implies a larger power consumption, the trade-off is solved by choosing the minimum current that copes with noise specifications. Sometimes this will leave electronic noise as the dominant term, especially in low-power consumer applications and especially when parasitic capacitances determine an unwanted noise amplification. Other times, especially in high-end applications, this will correspond to having electronic noise matched to thermomechanical noise.

Given the fact that the resistance R_F plays no role in the stage gain and offset, its spreads and drifts will minimally affect the stage behavior. Conversely, any spread in the value of the capacitances will imply a sensitivity spread from part to part. Additionally, if the capacitance value C_F drifts over temperature, this will directly turn into a temperature drift.

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Question n. 2

You are designing a novel pinned photodiode for pure black and white mobile imaging applications. Given the parameters in the table:

absorption coefficient @ 400 nm	$1.27 \cdot 10^7$ m^{-1}
absorption coefficient @ 650 nm	$1.95 \cdot 10^5$ m^{-1}
relative gate capacitance	6 fF/(µm)^2
minimum transistor width	150 nm
minimum transistor length	90 nm
floating diffusion depletion width	0.4 µm
minimum n^+ implant side	150 nm
minimum p^+ implant side	200 nm
minimum n^- diffusion side	2 µm
overall pixel size	3 µm x 3 µm
supply voltage	2.5 V

(i) sketch the photodiode structure, size the depth of the pinned implant and the thickness of the P-type epitaxial layer so to guarantee a quantum efficiency of 60% at 400 nm and of 85% at 650 nm;

(ii) verify whether the floating diffusion depletion capacitance can be designed to be less than 10% of the gate capacitance, and estimate the fill factor.

The camera features micro-lenses. Given a reset time of 50 us, a light integration interval of 9.9 ms, and a transfer gate activation slot of 50 us:

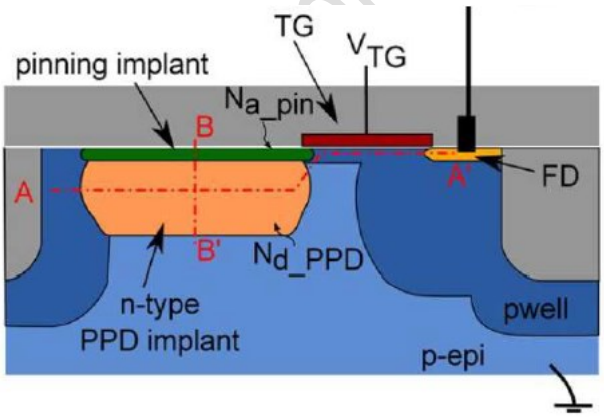
(iii) draw the voltage waveform at the floating diffusion node when an impinging photon flux of 10^{16} ph/s/m^2 at 650 nm hits the sensor. How would this waveform change when implementing correlated double sampling?

Physical Constants

$\varepsilon_{Si} = 11.7 \cdot 8.85\ 10^{-12}$ F/m

$k_b = 1.38\ 10^{-23}$ J/K;

$q = 1.6\ 10^{-19}$ C;



(i)

The structure is sketched above and it is formed by a buried pinned implant (N-type), separated from the surface through a thin, pinning, P+ implant. Aside we find the transfer gate that connects or isolates the PPD structures from the N+ type floating diffusion.

In order to guarantee a quantum efficiency of 60% at 400 nm we calculate the fraction of photons absorbed (i.e. lost) in the p-type implant and set it to 40%:

$$\eta_{400\,nm} = e^{-\alpha(\lambda_1)x_1} - e^{-\alpha(\lambda_1)x_2} = (1 - 0.6) = 0.4$$

with $x_1 = 0$.

Thus, the depth of the n-type implant is $x_2 = \frac{\ln\left(\frac{1}{0.6}\right)}{1.27 \cdot 10^7\ m^{-1}} = 40.22\ nm.$

To guarantee a quantum efficiency of 85% at 650 nm we calculate the number of photons absorbed in the epitaxial layer (they will be gathering by drift or diffusion within the pinned photodiode region):

$\eta_{650\ nm} = e^{-\alpha(\lambda_2)x_1} - e^{-\alpha(\lambda_2)x_2} = 0.85$

with $x_1 = 40\ nm$, that is the depth of the n-type region.

Thus, we find the epitaxial layer thickness $x_2 = \frac{\ln\left(\frac{1}{0.15}\right)}{1.95 \cdot 10^5\ m^{-1}} = 9.73\ \mu m \approx 10\ \mu m.$

(ii)

We want to verify whether the floating diffusion capacitance can be designed to be less than 10% of the gate capacitance. Assuming minimum dimensions for the transistor, the FD capacitance is given by:

$$C_{FD} = \epsilon_{Si} \cdot \frac{A}{d} \leq \frac{1}{10} \cdot 6 \frac{fF}{\mu m^2} \cdot 0.15\ \mu m \cdot 0.09\ \mu m$$

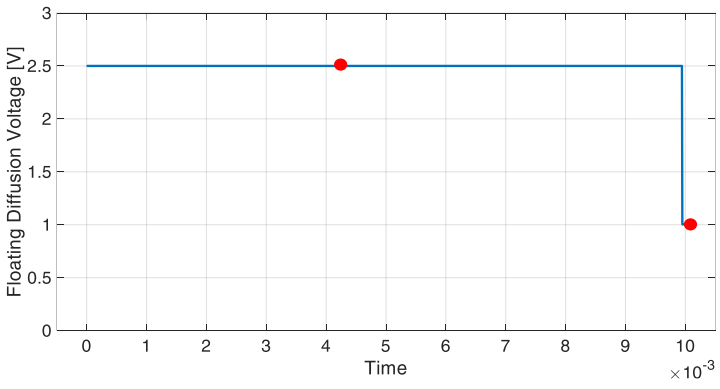
where *A* is the floating diffusion area, and *d* its depth. Requiring an area $A \leq (177\ nm)^2$, which copes with the minimum n^+ implant side specification. The Fill Factor, assuming all 4T with minimum dimensions and choosing a minimum FD area:

$$FF = \frac{(3\ \mu m)^2 - (150\ nm)^2 - 4 \cdot (150\ nm \cdot 90\ nm)}{(3\ \mu m)^2} \approx 99.15\ \%$$

Additionally, the presence of microlenses implies an almost 100% FF as far as the signal is considered.

(iii)

In a 4T configuration, the voltage at the floating diffusion node does not change during light integration in the PPD. It is rather updated only when the transfer gate is activated. The voltage waveform at the FD node is thus simply as shown aside.



And the voltage drop (during the transfer phase) is equal to:

$$\Delta V_{FD} = \frac{Q_{int}}{(C_{dep}+C_g)} \approx \frac{\Phi_{ph} \cdot t_{int} \cdot \eta_{650nm} \cdot FF \cdot A_{pixel} \cdot q}{C_g} = 1.49\ V$$

An operation of correlated double sampling does not alter the waveform at the FD node. It simply consists in sampling the FD voltage in the two points e.g. highlighted by the red markers and performing subtraction to remove possible reset noise.

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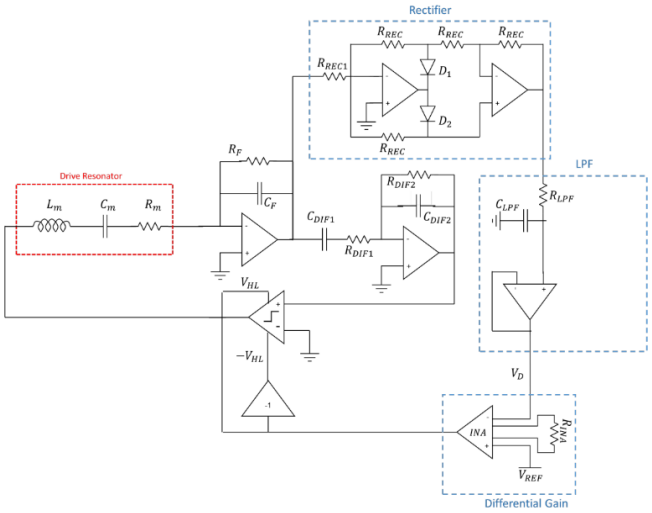
Question n. 3

drive detection transduction η_{DD}	220 nA/(m/S)
drive actuation transduction η_{DA}	20 nN/V
sense transduction η_S	3000 nA/(m/S)
supply voltage	±5 V
MOS overdrive voltage	300 mV
split between drive and sense	1.5 kHz
target resolution	2.5 mdps/√Hz
full-scale range	3000 dps
parasitic capacitance	6 pF

Consider the drive loop of a gyroscope operating at a resonance frequency of 50 kHz, as shown in the figure aside. Given the parameters in the table:

- **(i)** optimize the feedback capacitance and resistance of the drive-detection front-end stage and calculate the required reference voltage in the AGC loop to achieve a steady state oscillation with a 12 µm amplitude;
- **(ii)** knowing that the maximum peak current that can be delivered by the front-end stage is 2 µA, size the second stage such that, while providing a unitary gain, introduces a -90° lag to cope with the Barkhausen criteria for the entire loop.



Consider now the entire sense chain:

- **(iii)** draw the electronic building blocks up to the digital output and, neglecting thermo-mechanical noise, size the front-end feedback capacitance, the current drawn by each front-end MOS transistor and the required n. of bits of the ADC.

Physical Constants

$\varepsilon_0 = 8.85\ 10^{-12}$ F/m

$k_b = 1.38\ 10^{-23}$ J/K;

T = 300 K;

(i)

C_F and R_F are chosen in order to cope with the FSR requirement and to guarantee that the charge amplifier pole frequency is $f_p \ll f_0$:

$$\frac{1}{2\pi f_0 C_F} \cdot i_{DD} = \frac{1}{2\pi f_0 C_F} \cdot x_d \cdot 2\pi f_0 \cdot \eta_{DD} = VDD = 5\ V$$

$$C_F = 528\ fF$$

We choose: $f_p = \frac{1}{2\pi C_F R_F} = \frac{f_0}{100} = 500\ Hz \quad \rightarrow \quad R_F = 602.86\ M\Omega$

The voltage reference V_{REF} is set by the specification on the drive displacement:

$$V_{DD} \cdot \frac{2}{\pi} = V_{REF} \quad \rightarrow \quad V_{REF} = 3.18\ V$$

(ii)

At the resonance frequency in order to satisfy the Barkhausen conditions the second stage acts as a differentiator introducing a -90° phase lag.

The output current delivered by the front end sets the value of the capacitance C_{DIFF1} (the peak current occurs for the maximum slope of the sinewave with amplitude V_{DD}):

$$V_{DD} \cdot 2\pi f_0 \leq \frac{I_{OUT}}{C_{DIFF1}} \quad \rightarrow \quad C_{DIFF1} \leq 1.27\ pF$$

We choose $C_{DIFF1} = 1.27\ pF$.

The gain of the stage at the resonance frequency is

$$|G_{90D}(\omega_0)| = 2\pi f_0 \cdot R_{DIFF2} \cdot C_{DIFF1} = 1 \quad \rightarrow \quad R_{DIFF2} = 2.5\ M\Omega$$

Finally, we choose to set both the poles at a frequency 100 times larger than f_0.

$$\frac{1}{2\pi C_{DIFF1} R_{DIFF1}} = 100 \cdot f_0 \quad \rightarrow \quad R_{DIFF1} = 25\ k\Omega$$

$$\frac{1}{2\pi C_{DIFF2} R_{DIFF2}} = 100 \cdot f_0 \quad \rightarrow \quad C_{DIFF2} = 12.73\ fF$$

(iii)

The sense chain is composed by a charge-amplifier, a demodulation stage with low-pass filtering, and an ADC.

The feedback capacitance of the charge-amplifier is set by the FSR:

$$\frac{V_{DD}}{\Omega_{FSR}} = \frac{1}{2\pi f_0 C_F} \cdot \eta_S \cdot \frac{x_d}{\Delta\omega} \cdot \omega_d \quad \rightarrow \quad C_F = 42.4\ fF$$

(η_S is here assumed as the differential transduction. Otherwise the capacitance turns out to be twice the value above).

For the noise evaluation we reasonably consider R_F and thermo-mechanical noise negligible.

We can express the noise at the output of the CA considering two input transistors (or four if you considered differential sense read-out), then express it as input referred noise and compare it with the requirement:

$$\frac{\sqrt{2 \cdot \frac{4kT\gamma}{g_m}\left(1 + \frac{C_P}{C_F}\right)}}{\frac{\eta_S}{C_F}\frac{x_d}{\Delta\omega_{ds}}} \leq 2.5\frac{mdps}{\sqrt{Hz}} \cdot \frac{\pi}{180°}$$

$$\sqrt{2 \cdot \frac{4kT\gamma}{g_m}} = 56\frac{nV}{\sqrt{Hz}}$$

$$g_m = 7\ \mu A/V \rightarrow I = \frac{V_{ov} g_m}{2} = 1\ \mu A$$

(in case you assumed four transistors, the required current would be accordingly larger).

The number of bits is calculated from the dynamic range:

$$DR = 2^n = \frac{5V}{2.5\frac{mdps}{\sqrt{Hz}} \cdot \sqrt{\frac{\Delta f_{ds}}{3}} \cdot \left(\frac{5V}{3000\ dps}\right)} = 94.6\ dB$$

$$n = \log_2(DR) = 15.6$$

We thus choose an ADC with 16 bits (assuming an additional factor of 1/√12 for quantization noise would be fine as well).