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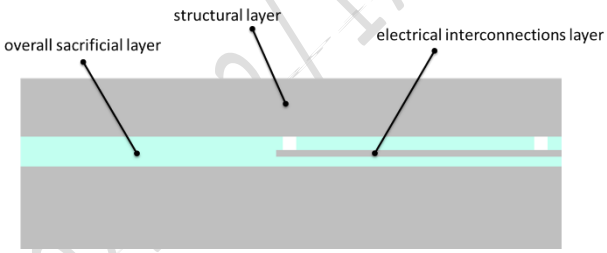
Question n. 1

Describe the four main steps of a typical MEMS microfabrication process: (i) the structural layer growth, (ii) the definition of the MEMS sensor shape, (iii) the structure release and (iv) the final packaging.

While describing the details of each of these four steps, please also highlight how the sensor parameters or performances are affected by the fabrication parameters.

A MEMS process has the goal of creating suspended microstructures, accessible through electrical signals. To this purpose, it is fundamental to obtain conductive, suspended parts, as well as interconnection electrodes and small gaps for capacitive sensing. Operation in vacuum, finally, enables damping and thus noise minimization.

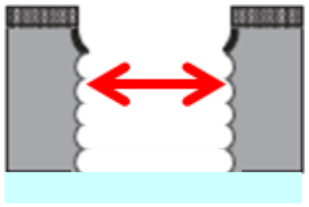
(i)



The first step, consisting in the structural layer growth, is usually performed through a procedure known as epitaxial growth, where a thick layer of polysilicon is formed by mixing a proper quantity of precursor gases in a chamber, properly heated and kept at the proper pressure. The overall thickness of the obtained layer, usually ranging in the 20-50 µm range, is fundamental for inertial sensors, as their intrinsic noise (NEAD and NERD), indeed, decreases with increasing mass values.

Also the thickness uniformity is relevant, as it affects the resonance frequency of out-of-plane modes, generating e.g. different sensitivity from part to part in z-axis accelerometers (due to the variability of the resonance frequency) and e.g. different sensitivity from part to part in pitch/roll gyroscopes due to different mode-split values from part to part.

(ii)

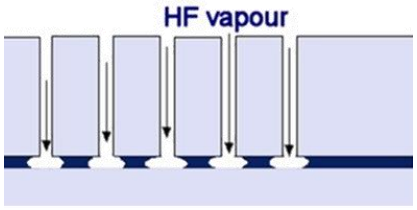


The second relevant step in the microfabrication is the structural layer etching, used to define the shape of the suspended parts. It is fundamental to reach a high form-factor, i.e. the possibility to have narrow and deep trenches. As a consequence, isotropic etching is not a good option. Anisotropic etching, instead, is the preferred option, usually obtained through a procedure known as Deep Reactive Ion Etching (DRIE), where a high-form factor (values around 30) can be obtained through the consecutive application of small isotropic etching (see the figure aside) with following protection of sidewalls, which determines, in the end, a quasi vertical etching.

The ability to reach small gaps is of paramount importance, as this sets the tranwsduction factor of capacitive driving and sensing: with lower gaps, the same motion at lower driving signals, ot larger sensing signals for the same motion, can be achieved. In turn, this is beneficial to reduce input-referred effects of electronic noise.

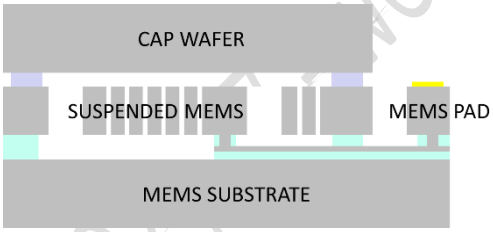
Once again, process repeatability is fundamental. Differences in etching from part to part may induce differences in resonance frequency (due to spring etching) and in transduction factor (due to gap etching). Additionally, local differences on the same structure may induce quadrature errors in gyroscopes. From this standpoint, also the sidewall orthogonality (so-called skew angle effect) is fundamental to avoid out-of-plane effects of drive forces in pitch/roll gyroscopes.

(iii)



Once the structural layer shape is defined, the polysilicon frames should be released. This is obtained by etching the sacrifical oxide underneath the structure through proper gases (e.g. HF vapour). This etching advances by a distance, underneath the structure (see the figure), which is proportional to the etching time: the step thus defines also the minimum width of the parts that shall remain anchored, which is also the maximum width of the suspended parts. Wherever a suspended frame should be larger than this width, holes in the frame should be positioned so to allow the correct release.

(iv)



Finally, packaging is used for a triple role of (a) protecting the structure from external dust, (b), setting the propoer operating pressure so adapt the Q factor to the specification requirements, and (c) forming an inert gas environment (e.g. Na or Ar) to avoid silicon oxidation during the device lifetime.

The step consists in bonding a CAP wafer on top of the MEMS wafer, where bonding is ensured by a proper material sealing the MEMS cavity (in light purple in the figure above): the material can be glassfrit (a sort of glass powder that melts at reasonablylow temperatures compared to metal melting temperatures) or an alloy of material that, under thermo-compression, metls to form the sealing.

Usually, a getter material (added in the cavity from the CAP side) is also used for devices that require low-pressure operation (in the mbar range or fractions thereoff, like gyroscopes). No getter is used for accelerometer, which operate at a slighlty larger pressure value (e.g. 10 mbar to 100 mbar).

Once more, repeatability of the package pressure from part to part is fundamental to ensure performance repeatabiilty of different structures: indeed, pressure influences the quality factor and in turn all the parameters that are a function of it (noise, ringdown time, bandwidth, motion amplitude…).

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Question n. 2

Working for an imaging company, you are asked by the Head of the Reverse Engineering Section to analyze a digital camera with the publicly available parameters reported in the table. In particular, the parameters are given for a video operation at 46 frame per second (fps):

Parameter [unit]	Value
Pixel side	5 µm
Frame rate	46 fps
Number of bits	12
Supply voltage	2.8 V
Sensor size	16.8 x 12.5 mm^2
Full Well Charge	15000 e^-
Conversion Gain	0.25 LSB/e^-
Signal independent noise	9.6 e^-_{rms}
Dark current	41.2 e^-/s
Dynamic Range	61.9 dB
Maximum SNR	41.3 dB
Power consumption	900 mW

(i) making and justifying reasonable assumptions on the pixel topology, verify the values of the conversion gain, of the full-well capacity, and of the signal independent noise, through the other parameters given in the Table;

(ii) with the same approach, verify the values of the dynamic range and of the maximum SNR;

(iii) estimate the maximum current flowing in each source follower.

Physical Constants

ε_0 = 8.85 10^{-12} F/m

k_b = 1.38 10^{-23} J/K;

T = 300 K;

q = 1.6 10^{-19} C;

(i)

Given the relatively limited DR, we start assuming that the pixel topology we are considering is of the 3-transistor type. Therefore, we can also assume that the integration capacitance will be dominated by the depletion capacitance, especially when the pixel area is relatively large as in this example. We thus assume a value for the integration capacitance given by:

$$C_{dep} = \frac{\epsilon_{Si} A_{px}}{x_{dep}}$$

Where the depletion capacitance can be calculated assuming a reasonable doping value of the depletion region. Using $N_A = 10^{15} cm^{-3} = 10^{21} m^{-3}$, and assuming a 0.7 V built-in voltage, we get for the maximum reverse bias:

$$x_{dep} = \sqrt{\frac{2\epsilon_{Si}(V_{rev} + V_{bi})}{q\, N_A}} = 2.1\, \mu m \quad \rightarrow \quad C_{dep} = 0.85\, fF$$

The integration capacitance will be likely slightly larger due to the gate capacitance, but we assume it as negligible given the large pixel area. Therefore, the conversion gain becomes:

$$CG = \frac{q}{C_{dep}} = 188 \frac{\mu V}{e^-}$$

Given the LSB:

$$LSB = \frac{V_{DD}}{2^{N_{bit}}} = 683 \frac{\mu V}{LSB}$$

We get a conversion gain in terms of LSB per electrons equal to: $CG = \frac{\frac{q}{C_{dep}}}{\frac{LSB}{e^-}} = 0.27 \frac{LSB}{e^-}$, which is reasonably close to the value given in the table. We note that probably the gate capacitance slightly increases the total integration capacitance, thus decreasing accordingly the conversion gain to the value indicated in the table. This confirms that our assumptions were correct.

For what concerns the full-well charge, as we know the approximate integration capacitance value and the biasing voltage, for a 3T configuration we just have:

$$FWC = \frac{C_{dep} V_{DD}}{q} = 14900\ e^-$$

The value is very close to the one reported in the table.

Finally, to cross-check values of noise we need to make an assumption on the integration time. As we are given the frames per second, we can reasonably assume that most of that time is used for integration (in a 3T operation, reset time and readout time are negligible compared to the integration time). Assuming thus $t_{int} = \frac{1}{46\ fps} = 21.7\ ms$, for a dark current given as $i_d = q \cdot 41.2 \frac{e^-}{s} = 6.6\ aA$ (a very low value), we get a total signal-independent noise given as:

$$\sigma_{si} = \frac{\sqrt{q i_d t_{int} + k_B T C_{dep}}}{q} = 11.7\ e^-_{rms}$$

which is in line with the value given in the Table.

All our assumptions on the 3T topology are thus valid.

(ii)

For what concerns DR and maximum SNR, as we are dealing with a 3T topology, calculations are straightforward. We indeed get:

$$DR = 20 \log_{10} \frac{FWC}{\sigma_{si}} = 20 \log_{10} \frac{15000}{9.6} = 63.9\ dB$$

Using the parameters calculated at point (i) above would have yielded a very similar result, which matches the one indicated in the Table. Additionally, we can write that the maximum SNR is limited by Poisson (assuming negligible PRNU), so to get:

$$SNR_{max} = 20 \log_{10} \sqrt{FWC} = 41.7\ dB$$

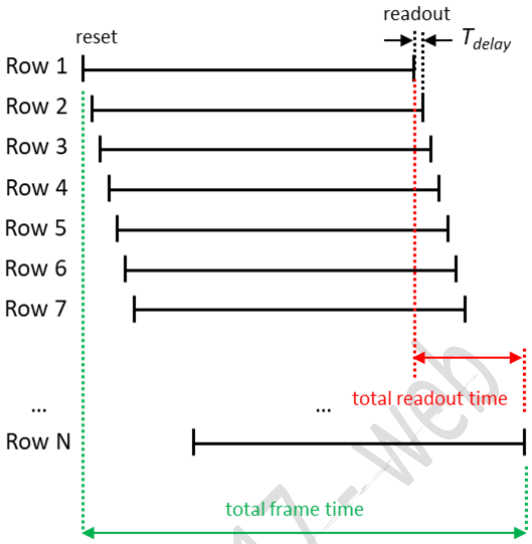
Which matches the value in the Table.

(iii)

The dominant portion of the overall power consumption will be generated when the source follower transistors are activated for the readout phase. To understand the maximum current flowing in each source follower, assuming a rolling shutter readout, we thus need to:

- split the overall power consumption among the number of current generators, i.e. one per column: $P_{gen} = \frac{P_{tot}}{N_{col}} = \frac{P_{tot}}{(L_{sensor}/L_{pixel})} = \frac{900\ mW}{(12.5mm/5\mu m)} = 360\ \mu W$;

- calculate the corresponding average current during operation, considering that the source follower is biased at V_{DD}: $i_{av,gen} = \frac{P_{gen}}{V_{DD}} = 128\ \mu A$;
- assume that the total readout time (i.e. the time to complete the rolling shutter readout, which is the distance between the end of the first row readout to the last row readout) will be a reasonable fraction of the total frame time. As the frame time is 21.7 ms, we can assume e.g. a readout time of 1/5 of this value. As a consequence, the current calculated above will be the average between 4/5 of zero current (source follower off during reset and integration) and 1/5 of maximum current, i.e. a duty cycle of 1/5. We thus get a maximum current corresponding to: $i_{max,gen} = \frac{i_{av,gen}}{duty_{cycle}} = 640\ \mu A$.



This current value appears to be a bit larger than typical biasing current of few μA to few 10s μA. Likely, the sensor is consuming more power due to digital processing, but we have no elements to properly infer the consumption distribution between analog operation and digital operation. We have thus no elements for a correct reverse engineering on this side.

Note that assuming 1/5 of readout time, the actual integration time used in the points above should be reduced to 17.5 ms… which however would not cause a big difference in the calculations.

Note: this exercise lends to multiple approaches to the solution, so to stimulate students express their knowledge. If you solved the exercise in a different way, but with coherent reasoning and correct considerations, that was considered positively!

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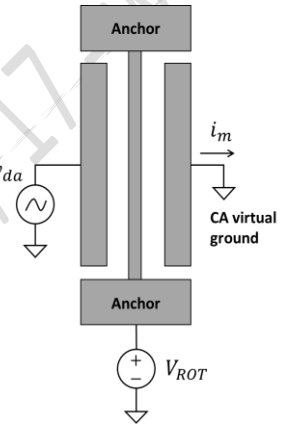
Question n. 3

Young's modulus	E	160 GPa
Polysilicon density	ρ	2330 kg·m^{-3}
Process height	h	100 µm
Parallel plate length	L_{PP}	160 µm
Minimum gap	g	2 µm
Rotor bias voltage	V_{ROT}	10 V
Nominal resonance	f_0	524 kHz
Linearity error	ϵ_{lin}	5%
Process error	σ_x	10 nm
Clock frequency	f_{ck}	32768 Hz
Op-amp max output	$V_{o,max}$	± 2.5 V

Your task is to design a MEMS clock to be used as a time-base for wearable applications. The clock output frequency should be 32768 Hz (i.e., 2^{15} Hz), but it is obtained starting from a higher MEMS resonance frequency value of 524 kHz.

To save area, the MEMS resonating element is implemented as a clamped-clamped beam actuated and sensed by parallel plates as in the figure. The oscillator is implemented as in the scheme below, with a unity-gain phase shifter and a comparator implemented by a high-gain INA stage.

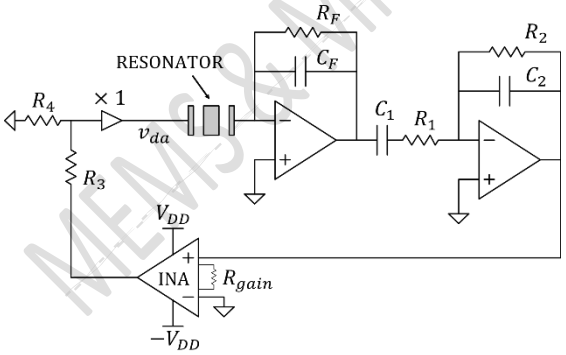


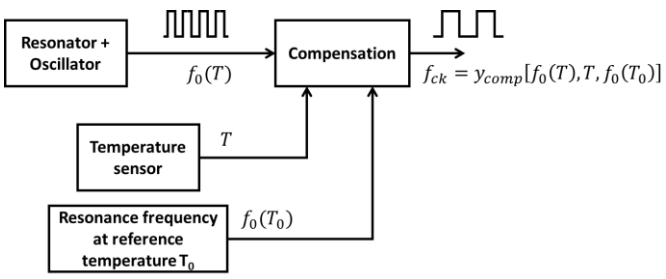
(i) Calculate the beam width to obtain the nominal resonance frequency f_0 at room temperature (*hint*: consider all the beam mass concentrated on the central point). Neglect electrostatic softening in the calculations but assess its impact at the end.

(ii) Size the feedback capacitance C_F of the charge-amplifier, knowing that the rotor displacement should be limited to keep the linearity error of the single-ended capacitive sensing within 5%. Qualitatively, sketch the transfer function of the phase shifter (modulus and phase), clearly highlighting the position of the MEMS resonance frequency in the graph (sizing of passive components is not required).

A compensation of errors in the mechanical frequency is performed by means of a system-level architecture, where the Compensation element should automatically perform a frequency division by the required factor. The system includes a temperature sensor to monitor temperature variations, and it is subject to an initial calibration of the nominal frequency at ambient temperature T_0 = 300 K.

(iii) Consider now the effect of process spreads and temperature on the resonance frequency, considering errors on in-plane etching characterized by $\sigma_x = 10$ nm. First, calculate the worst-case variation of resonance frequency, considering a 3-σ variation of the beam dimensions. Secondly, write the function y_{comp} that the compensation block needs to implement to obtain the desired output frequency (32768 Hz), compensating both temperature and process-induced errors.





Physical Constants

ε_{Si} = 8.85 10^{-12}·11.7 F/m
k_b = 1.38 10^{-23} J/K;
T = 300 K;

(i)

The resonance frequency of the beam can be approximated by considering the usual formula, where the stiffness is the one of a clamped-clamped beam (i.e. two guided-end beams in parallel), and the mass is assumed concentrated in the mid-point:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k_{mech}}{m}} = \frac{1}{2\pi}\sqrt{\frac{2 \cdot 2 \cdot \frac{Ehw^3}{(L/2)^3}}{\rho hwL}} = \frac{1}{\pi}\sqrt{\frac{8Ew^2}{\rho L^4}}$$

The stiffness is multiplied by an additional factor 2 in order to account for the average beam displacement (equivalent to having twice the stiffness), instead of the displacement of the mid-point which is maximum (same consideration as for magnetometers springs). Inverting the formula, and taking, for the sake of simplicity, the beam length equal to the parallel plates length:

$$w = \pi f_0 L^2 \sqrt{\frac{\rho}{8E}} \approx 1.8\ \mu\text{m}$$

The equivalent electrostatic stiffness (also multiplied by a factor 2) is:

$$k_{elec} = -2 \cdot \frac{2V_{ROT}C_0}{g^2} = -7.08\frac{N}{m}$$

And it is much smaller than the mechanical stiffness $k_{mech} = 726.6\frac{N}{m} \approx 0.01|k_{elec}|$. Including softening, the resulting resonance frequency is:

$$f_0 = \frac{1}{2\pi}\sqrt{\frac{k_{mech} + k_{elec}}{m}} = 521.44\ \text{kHz}$$

(ii)

The maximum displacement that complies with the linearity error for the single-ended sense capacitance variation is:

$$\epsilon_{lin} = \frac{x_{max}}{g} \;\Rightarrow\; x_{max} = g\epsilon_{lin} = 100\ \text{nm}$$

Given the transduction coefficient:

$$\eta = V_{ROT}\frac{C_0}{g} = V_{ROT}\frac{\epsilon_0 h L_{PP}}{g^2} = 3.54 \cdot 10^{-7}\frac{\text{VF}}{\text{m}}$$

The output of the charge-amplifier reaches the maximum limit $V_{o,max}$ with a feedback capacitance equal to:

$$C_F = \frac{\eta x_{max}}{V_{o,max}} = 14.16\ \text{fF}$$

Let's now focus on the phase shifter: the resonator introduces 0° phase shift from voltage to current, the charge amplifier introduces -270°, the comparator does not invert the signal, thus -90° are needed. The stage needs to operate as an inverting differentiator, hence the poles should be placed at least a decade after the nominal frequency (e.g. $f_p = 5.24\ \text{MHz}$ or $f_p = 52.4\ \text{MHz}$). The corresponding plot, with the working point highlighted, is shown in the figure below.

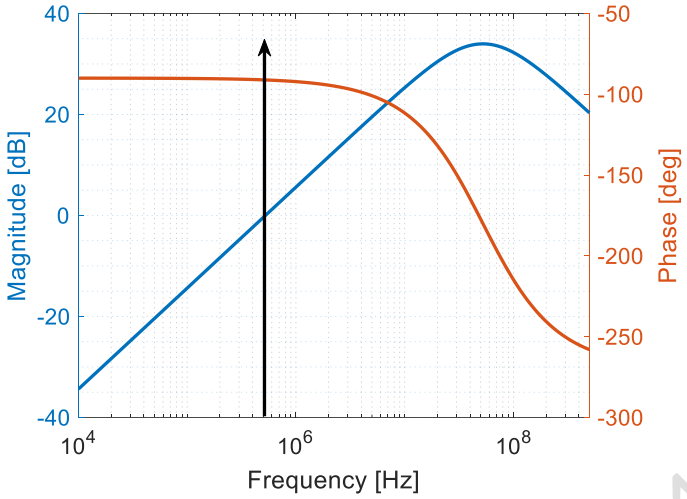


Figure 1. *Bode plot of the phase shifter stage.*

(iii)

Etching non-uniformity affects both the stiffness and the mass of the beam. Linearizing the expression of the resonance frequency, and considering a 3-σ variation of both the sides of the beam (thus 6-σ for the beam width), the total variation due to a variation of the width is:

$$\frac{df_0}{f_0} = \frac{1}{2}\frac{dk}{k} - \frac{1}{2}\frac{dm}{m} = \frac{3}{2}\frac{dw}{w} - \frac{1}{2}\frac{dw}{w} = \frac{dw}{w} = \frac{6\sigma_x}{w} = 3.34\%$$

Such variation will result in a statistical variation of the resonator nominal frequency within the value above, also described as “process offset”. This variation is indeed fixed once the device is fabricated, and its effect can be evaluated by performing an initial characterization of the device at a known temperature T_0 (usually room temperature), yielding the true resonance frequency $f(T_0)$:

$$f_0(T_0) = \overline{f_0} \cdot (1+\beta) = 524\ kHz \cdot \left(1 + \frac{\overline{dw}}{w}\right)$$

On top of such offset, temperature variations of the environment will induce a variation of the resonance frequency around this value, characterized by the linear temperature coefficient of $\alpha_f = -30$ ppm/K. As a result, the output frequency of the oscillator is described by the following expression:

$$f_0(T) = f_0(T_0)\left(1 + \alpha_f(T - T_0)\right)$$

The temperature sensor within the system enables measuring the T variation with respect to the reference temperature, and thus it allows compensation of the reference frequency. As the output frequency needs to be much smaller than the nominal frequency, the function y_{comp} is a frequency division:

$$y_{comp}\big(f_0(T),\ T,\ f_0(T_0)\big) = \frac{f_0(T)}{N\big(T, f_0(T_0)\big)} = \frac{f_0(T)}{\left(1 + \alpha_f(T - T_0)\right)} \cdot \frac{524\ kHz}{f_0(T_0)} \cdot \frac{1}{16}$$

Where the temperature-and-process-dependent division factor $N\big(T, f_0(T_0)\big)$ is:

$$N\big(T, f_0(T_0)\big) \approx \underbrace{\left(1 + \alpha_f(T - T_0)\right) f_0(T_0)}_{\text{Process/Temperature compensation}} \cdot \underbrace{\frac{16}{524\ kHz}}_{\text{Nominal division modulus}}$$