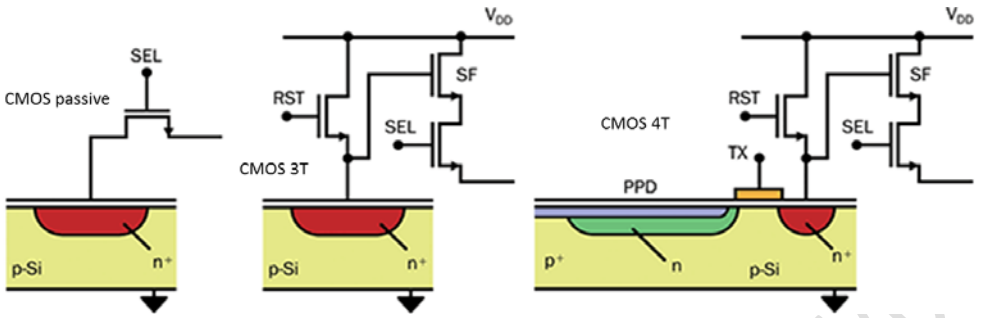
Last Name ___Son_____ **Given Name** ____Dolores____ **ID Number** ___20170703___

Question n. 1

The history of CMOS image sensors has seen two major breakthroughs in passing from passive to active pixels (APS), and then in passing from 3T to 4T APS. First describe the operation of the 3T topology, highlighting advantages and drawbacks against the passive one. Then describe the operation of the 4T topology, highlighting advantages and drawbacks against a 3T solution. You may use graphs to assist your discussion.



A **passive CMOS pixel** is formed just by a photodiode (PD) plus a selection transistor. While this implementation maximizes the fill-factor (FF ~ 1), it does not provide a "usable" charge-to-voltage conversion at pixel level. This is easily shown: assume that the pixel is first reset at V_{DD}, and then left floating for integration; though during charge integration a voltage arises across the photodiode capacitor, there is no low-impedance voltage-driving capability. For large matrixes, with large parasitic load capacitance at each column, such a pixel selection (for the readout) would results just in a charge sharing of the photodiode charge to the column capacitances, without consistent change in the voltage at the column preamplifier input. For passive-pixels, the only viable way is indeed to use other charge transfer mechanisms, like in CCDs.

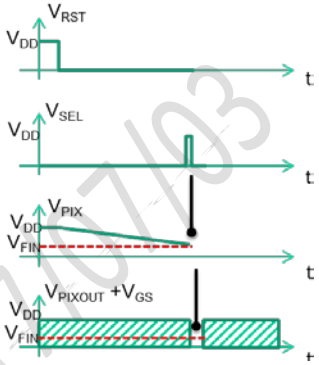
The **3T APS** topology solves the problem of passive CMOS pixels by providing an in-pixel charge-to-voltage conversion with low-impedance voltage output. This is achieved by using a source follower (SF) configuration that buffers the voltage at the photodiode (PD) anode, giving capabilities to drive also large capacitances affecting the columns to the output column amplifiers/ADCs. A 3T APS configuration works in three main phases:

- **reset**: during this phase, the gate of the reset (RST) transistor is kept high, so that the anode is reset to about V_{DD}. Any photo or dark current flows between ground and V_{DD}. Note that with values in the sub-pA range, the anode voltage remains close to V_{DD} even for non-negligible (e.g. few kΩ) nMOS on-resistance. In this phase, the selection (SEL) nMOS is off (gate low), so the SF is off as well. The pixel output is not valid (not connected to the column output);

- **integration**: the opening of the RST transistor indicates the transition between the reset phase and the integration phase. With RST off, the photo and dark currents now can only flow directly across the capacitance affecting the anode node (PD depletion capacitance, C_{PD}, plus parasitic at the SF gate, C_G). For this reason, this kind of charge collection is known as direct integration. As a consequence of the integration, the voltage, initially preset at V_{DD}, begins to drop. Note that the drop is not linear, as C_{PD} itself is a function of the voltage across it (the larger the photodiode capacitance compared to the parasitic at the SF input, the larger the nonlinearity). The conversion from charge to voltage is regulated by a conversion gain (C_G) determined by the sum of the PD and parasitic capacitances, $C_{PD} + C_G$. If during the integration time the accumulated charge drop exceeds a value of about $(C_{PD} + C_G)V_{DD}$, then saturation occurs. Also in

this phase, the SF transistor is not biased by the SEL transistor (note: therefore it thus not dissipate power) and the column output is not determined by the specific pixel we are considering;

- **readout**: the rising in the SEL gate voltage indicates the transition from the integration to the readout phase. As SEL is now high, the column current generator biases the SF transistors, which can buffer to its source (i.e. now the column output) the voltage at its gate. As the SF is a low-impedance output stage, it can easily drive large capacitive loads in relatively fast times, thus enabling high-frame rate, readout. This definitely enables a full-resolution, fast scanning of matrixes of several Mpixels. The figure summarizes the evolution of voltage signals across the most significant nodes in the 3T topology.



Though all its advantages compared to passive solutions, the 3T APS shows a dynamic range that typically does not exceed 60 dB, far from values of silver halide analog films. Limits are given by the relatively large dark current (and associated shot noise), due to surface-generated dark charges at the dirt Si-SiO_2 interface. Additionally, reset noise introduced by thermal noise of the RST on-resistance, frozen at the beginning of the integration, is another limit to the DR.

The **4T APS** aims at solving the few, yet relevant, drawbacks of the 3T APS. This is elegantly accomplished by adding just one gate (transmission gate, TG) and a shallow surface P-implant to the 3T topology, as shown in the figure. The shallow-P/N/P-substrate region is known as pinned photodiode, as the P-type implant pins (blocks) the N-type deeper implant from the surface, and thus avoids collection of surface-generated dark charges. This solves the issue related to the dark current shot noise, mentioned above for 3T topologies.

In details, the operation of a 4T topology is similar to the 3T APS for the reset phase (PPD empty, TG is open and the floating diffusion is reset to V_{DD}), and for integration, except that charge is integrated on the PPD and not on the floating diffusion. At the end of the integration time, charge is transferred to the FD by closing the TG. At this point, there is a drop in the voltage across the FD (or, equivalently, at the gate of the SF), which is linear with charge, as the FD capacitance is dominated by the SF gate capacitance C_G, at 1st-order independent of the voltage across it. The readout operation is then identical to the 3T topology, with the SEL transistor biasing the SF, which buffers the voltage drop to the column output.

The additional, huge advantage of this 4-phase readout scheme, based on PPD+TG+3T to form the 4T APS, is that, during the integration, the reset voltage can be sampled (without signal) nondestructively by activating the SEL and SF transistors, and stored. After the readout phase described above, one can subtract the stored value to cancel electronic offsets and kTC noise.

Last but not least, the RST, SF and SEL transistors can be shared among different TG+PPD elements, to form compact overall pixels with, on average, a lower number of transistors per photo-element (e.g. 1.75T, with 4 TG+PPD, 1 RST, 1 SEL and 1 SF). This is particularly appreciated for ultra-compact sensors (e.g. mobile imaging).

On the other side, as large sensing areas (PPD) can be formed without affecting the CG (now dependent on C_G), this topology is well suited also for large-area, high-DR, high-end sensors.

Last Name ___Son_____ **Given Name** ____Dolores____ **ID Number** ___20170703___

Question n. 2

You have to design a consumer parallel-plate capacitive accelerometer. The most relevant specifications of the device and electronics are listed in table 1. You are asked to:

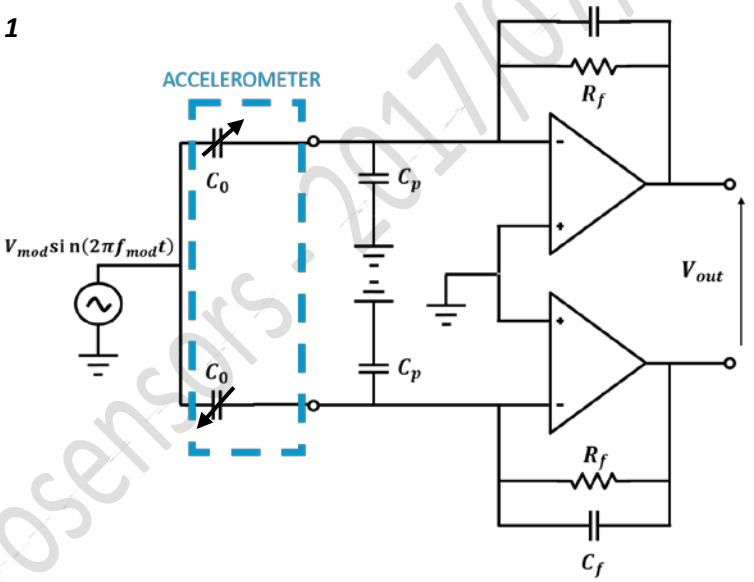
- **(i)** evaluate the mechanical stiffness of the accelerometer;
- **(ii)** estimate a range for the device intrinsic NEAD (*Noise Equivalent Acceleration Density*), making reasonable assumptions in case of unknown parameters;

You then decide to build a discrete-component circuit for device characterization (as in the figure below).

- **(iii)** starting from the performance reported in the three proposed datasheets, motivate in detail which operational amplifier you pick for the test.

Table 1

Parameter	Symbol	Value
Device mass	m	$5\ nKg$
Parallel plates (PP) length	L_{pp}	$300\mu m$
N. of differential PP cells	N_{pp}	8
Process height	H	$24\ \mu m$
Minimum gap	g	$1.5\ \mu m$
Feedback capacitance	C_f	$1\ pF$
Rotor modulation frequency	f_{mod}	$50\ kHz$
Rotor modulation amplitude (peak)	V_{mod}	$1\ V$
Required full scale range	FSR	$16\ g$
Acceptable linearity error	$\epsilon_{lin,\%}$	1 %



LME497RM		
Parameter	**Typical**	**Max.**
Input Voltage Noise	$2.7\ \frac{nV}{\sqrt{Hz}}$	
Input bias current	$10\ nA$	$75\ nA$
Supply Voltage		$\pm 2V$
Offset Voltage	$2mV$	$5mV$
Slew Rate	$15\ \frac{V}{\mu s}$	$20\ \frac{V}{\mu s}$
Parasitic capacitance	$5\ pF$	

AD86518		
Parameter	**Typical**	**Max.**
Input Voltage Noise	$2.7\ \frac{nV}{\sqrt{Hz}}$	
Input bias current	$1\ pA$	$10\ pA$
Supply Voltage		$\pm 1.8V$
Offset Voltage	$250\mu V$	$500\mu V$
Slew Rate	$10\ \frac{V}{\mu s}$	$15\ \frac{V}{\mu s}$
Parasitic capacitance	$16\ pF$	

AD80630		
Parameter	**Typical**	**Max.**
Input Voltage Noise	$7\ \frac{nV}{\sqrt{Hz}}$	
Input bias current	$10\ pA$	$60\ pA$
Supply Voltage	$\pm 1.8V$	
Offset Voltage	$500\mu V$	$1mV$
Slew Rate	$105\ \frac{V}{\mu s}$	$160\ \frac{V}{\mu s}$
Parasitic capacitance	$4\ pF$	

Physical Constants

q = 1.6 10^{-19} C
k_b = 1.38 10^{-23} J/K
T = 300 K (if not specified)
ε_0 = 8.85 10^{-12} F/m

(i) first of all, starting from the linearity error specification, the maximum displacement that the structure (based on a differential PP readout scheme) can undergo can be calculated:

$$x_{lin1\%} = g \cdot \sqrt{\frac{\epsilon_{lin,\%}}{100}} = 150nm$$

Then, the accelerometer resonant frequency can be easily determined by forcing the condition that the displacement at the full-scale does not exceed the maximum displacement that copes with linearity specifications, as found above:

$$\frac{x_{lin1\%}}{a_{FSR}} = \frac{1}{\omega_0^2} \quad \rightarrow \quad \omega_0 = \sqrt{\frac{a_{FSR}}{x_{lin1\%}}} \quad \rightarrow \quad f_0 = 2\pi\omega_0 = 5.1kHz$$

Knowing the mass, the total stiffness (sum of the mechanical and of the electrostatic ones) is readily obtained:

$$k_{tot} = \omega_0^2 m = 5.23\ N/m$$

In order to obtain the mechanical stiffness, we need to find and subtract the electrostatic contribution. This is a 'not-standard' situation: a variable voltage is applied to the rotor, while the stators are grounded. We can start from the expression of the electrostatic force and do some calculations:

$$F_{elec} = \frac{V(t)^2}{2}\frac{dC}{dx} = \frac{V_{MOD}^2 \sin^2(2\pi f_{mod} t)}{2}\frac{dC}{dx} = \frac{\frac{V_{MOD}^2}{2}(1 - sin(2\pi 2 f_{mod} t))}{2}\frac{dC}{dx}$$

We can distinguish a DC term and a $2f_{mod}$ term. The former is useful for our k_{el} computation; the latter is sufficiently higher than the resonance frequency and, consequently, it does not excite the device and can be neglected. Hence, we are interested in the following contribution:

$$F_{elec} \sim \frac{V_{mod}^2}{4}\frac{dC}{dx}$$

That results in an electrostatic stiffness equal to:

$$k_{elec} = -\frac{2C_0}{g^2}\left(\frac{V_{mod}}{\sqrt{2}}\right)^2 = -\frac{2\epsilon_0 H L_{pp} N_{pp}}{g^3}\left(\frac{V_{mod}}{\sqrt{2}}\right)^2 = -0.15\ N/m$$

In the end we can evaluate the mechanical stiffness, as requested:

$$k_{mech} = k_{tot} - k_{el} = 5.38\ N/m$$

(ii) as we are dealing with a consumer accelerometer, we should know that is reasonable to assume quality factors in a range between 0.5 and few units. Consequently, we can calculate a range of NEAD (e.g. for $Q = 0.5 \div 3$):

$$NEAD = \sqrt{\frac{4k_B T\omega_0}{Q\ m}} \sim 50 \div 20\ \ \mu g/\sqrt{Hz}$$

(iii) to answer this question, it can be useful to compute the overall sensitivity (input acceleration to output voltage). The expression for an accelerometer with a modulated voltage on the rotor is (for the expression derivation, see E02 Accelerometer Readout class):

$$S = \frac{\Delta V_{out}}{\Delta a_{ext}} = \frac{1}{\omega_0^2}\frac{2C_0}{g}\frac{V_{mod}}{C_f} = 4.2\ mV/g$$

Let us now take a look at the proposed datasheets: we can easily note that slew rate and offset voltages are not critical limitations in our situation. Indeed, offset is filtered thanks to signal modulation, while the maximum slope of a 50-kHz sinewave spanning the full-voltage dynamic of any of the chosen amplifiers copes with the given slew rates.

For what concerns, instead, the input bias current parameter, we can note some issues: this DC contribution flows into the feedback resistance and gives a DC output. If this does not cause signal saturation, we will be able to filter it, just like for the offsets above. However, if this contribution is such that the saturation of the amplifier can occur, then the readout will be compromised.

To find a range of possible values for the feedback resistance, we should make some considerations on the circuit transfer function: our feedback resistance, at least, should be high enough to set a pole one decade before our operating frequency, so to properly work in the capacitive feedback condition (charge amplifier):

$$R_{f,min} = \frac{1}{2\pi C_f 10 f_{mod}} = 32\ M\Omega$$

The huge bias current of the LME49FRM operational amplifier, in this case, cause a DC output voltage:

$$V_{out} = R_f i_{bias} = 32M\Omega \cdot 75nA = 2.3V$$

A value that exceeds the maximum power supply of the amplifier of 2V: the opamp is outside its linear region and the circuit does not work. Note that any higher values for R_f, which would give better noise performance for the circuit, would be even worse for this specific amplifier. We thus have to discard LME49FRM for bias current issues.

AD68518 and AD80630 have not critical bias currents, but we can compare them in terms of noise. Apparently, AD68518 has a lower input referred noise. However, we should keep in mind that this noise is brought to the output through the parasitic capacitance at the input node.

Let us evaluate the input referred acceleration noise densities for the two amplifiers:

$$S_{in,AD68518} = \frac{\sqrt{2 \cdot S_{v,opamp} \cdot \left(1 + \frac{C_P}{C_F}\right)^2}}{S} = \frac{\sqrt{2 \cdot \left(2.7\frac{nV}{\sqrt{Hz}}\right)^2 \cdot \left(1 + \frac{16pF}{1pF}\right)^2}}{S} = 15.3\ \mu g/\sqrt{Hz}$$

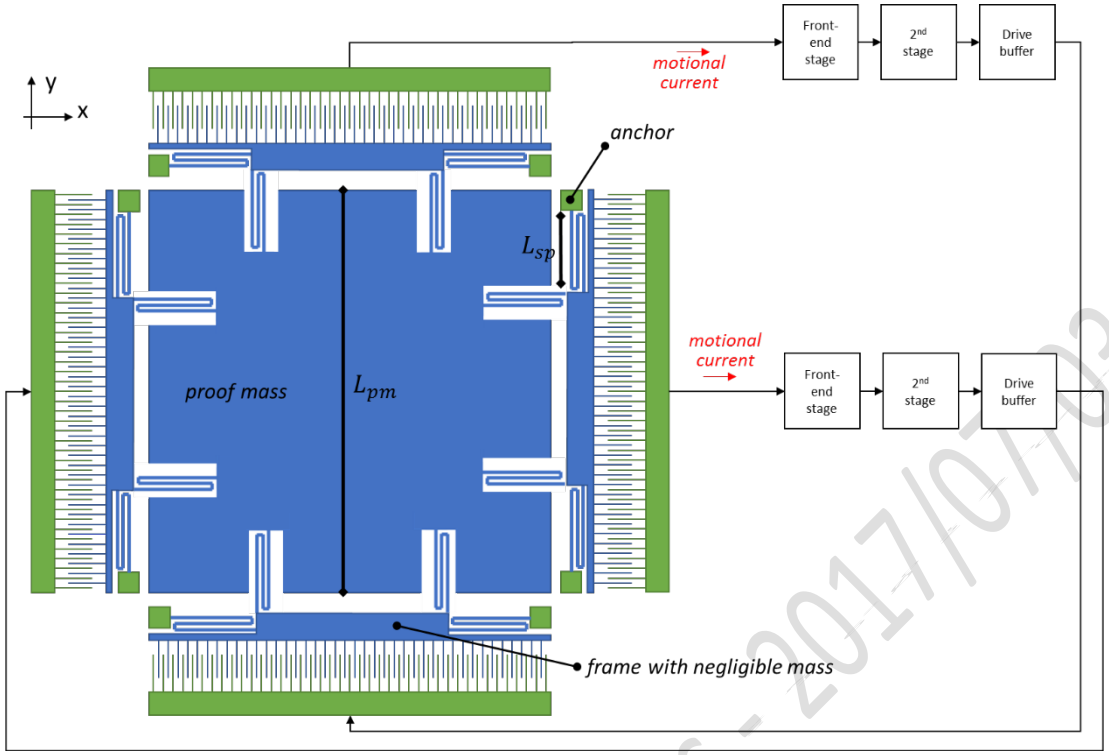
$$S_{in,AD80630} = \frac{\sqrt{2 \cdot \left(7\frac{nV}{\sqrt{Hz}}\right)^2 \cdot \left(1 + \frac{4pF}{1pF}\right)^2}}{S} = 11.6\ \mu g/\sqrt{Hz}$$

AD80630 is better in terms of noise, so we can pick this component for our readout circuit.

Note: the final two letters in the codes of the amplifiers were a suggestion for you, to choose the right one! 30 is better than 18, which is better than "rimandato".

Last Name ___Son_____ **Given Name** ____Dolores____ **ID Number** ___20170703___

Question n. 3



The figure shows a MEMS structure, fabricated in a 24-um thick process. The process allows a minimum gap of 2 um, and a minimum Poly-Si width of 2 um, as well.

The structure has two main resonance modes, for which the mass, actuated and sensed through comb fingers, displaces along the x and y directions. In detail, eight springs connect the anchors to four frames with negligible mass, and eight springs decouples the main proof mass from the four frames.

Each spring has three folds with a length L_{sp} equal to 50 µm. For each mode, 8 springs contribute to determine the mode stiffness. The proof mass can be approximated to a Silicon (density 2320 kg/m^3) square with 700 µm side (L_{pm}). Each resonator shows a quality factor of 10 000.

The two resonators are simultaneously forced to oscillate at resonance, by building an electronic oscillator around each of them. The drive buffer circuit delivers a square-wave that toggles between 0 and V_{UP} = 2 V.

The desired resonance of both resonators is 29 kHz. The desired motional current amplitude, i.e., the AC amplitude of the sinusoidal current that flows through the motion-detection port is 50 nA. You are asked to:

- **(i)** find the required spring width to match the desired resonance frequency;
- **(ii)** after maximizing the number of comb fingers of each electrode, find the required DC voltage on the rotor to have the desired motional current amplitude;
- **(iii)** find the displacement amplitude;
- **(iv)** develop the sustaining electronic loops, by sketching in details a circuit that forces identical velocity amplitudes of the motions of the two modes;
- **(v)** find the trajectory of the proof mass if a 90-deg phase shift is forced between the two drive buffers.

Physical Constants

q = 1.6 10^{-19} C
k_b = 1.38 10^{-23} J/K
T = 300 K (if not specified)
ε_0 = 8.85 10^{-12} F/m

The mass of each resonator is equal to the mass of the proof mass, that can be evaluated as

$$m = L_{pm}^2 * h * \rho_{PolySi} = 27.3 \text{ nkg}$$

Given the desired resonance frequency, 29000 Hz, the required stiffness of each resonator is thus

$$k = (2\pi f_r)^2 * m = 905 \text{ N/m}$$

Since each resonator is suspended with 8 springs, and since each spring is composed of a series of 3 folded beams, the required stiffness of a single beam is

$$k_{sb} = k * \frac{3}{8} = 339 \text{ N/m}$$

As

$$k_{sb} = E \frac{w^3 h}{L^3}$$

the required beam width is

$$w = L\left(\frac{k_{sb}}{Eh}\right)^{1/3} = 2.23 \text{ µm}$$

The amplitude of the fundamental harmonic of a $0 - V_{UP}$ square-wave is

$$v_a = \frac{4}{\pi}\frac{V_{UP}}{2}$$

As $V_{UP} = 2$ V, then, $v_a = 1.27$ V.

Since the desired motional current amplitude is 50 nA, the motional resistance of the resonator should be

$$R_m = \frac{v_a}{i_a} = 25.4 \text{ MΩ}$$

The damping factor can be estimated from the Q-factor as

$$b = m * \frac{2\pi f_r}{Q} = 497 \text{ nN/(m/s)}$$

As

$$R_m = \frac{b}{\eta^2}$$

the required η coefficient is $\eta = 149 \text{ V} * \text{fF/µm}$..

η depends on the capacitance variation per unit displacement of the electrodes and on the DC voltage between the rotor and the stators.

The capacitance variation per unit displacement can be found by maximizing the number of comb fingers per each electrode. As the comb finger pitch is twice the minimum PolySi width plus twice the minimum gap, i.e.,

$$p_{CF} = 2 * w_{min} + 2 * g = 8\ \mu\text{m}$$

the maximum number of comb fingers per electrode is

$$N_{CF} = \text{round}\left(\frac{L_{pm}}{p_{CF}}\right) = 87$$

Hence, the capacitance variation per unit displacement is

$$\frac{\partial C}{\partial x} = \frac{2 * \varepsilon_0 * h * N_{CF}}{g} = 18.9\ \text{fF}/\mu\text{m}$$

The rotor-to-stator DC voltage must thus be

$$V_{DC} = \frac{\eta}{\frac{\partial C}{\partial x}} = 7.5\ \text{V}$$

In these conditions, the displacement amplitude is

$$x_a = v_a \eta \frac{Q}{k} = 1.96\ \mu\text{m}$$

As the required control is on the velocity of the resonator, we can implement a TRA-based front-end, whose output is proportional to the motional current, hence to the velocity of the proof mass. The output of the TRA can be rectified, low-pass filtered, compared with a reference voltage, amplified and suitably connected with the driving circuitry to implement an AGC that controls the velocity, as desired. To have the same velocity amplitudes on both resonators, the two oscillators must have the same, identical sustaining loop, with the same AGC reference voltage.

As

$$x(t) = x_a \sin\big(\phi(t)\big)$$

and

$$y(t) = x_a \sin(\phi(t) + 90°) = \cos\big(\phi(t)\big)$$

the proof mass will orbit following a circular trajectory.